REMARKS

Applicants have studied the Office Action dated October 4, 2002, and have made amendments to the claim. Claim 1 is pending and has been amended. It is submitted that the application, as amended, is in condition for allowance. Reconsideration and reexamination are respectfully requested.

The Examiner objected to the Abstract of the Disclosure. Applicants have amended the Abstract of the Disclosure in accordance with the Examiner's remarks. A substitute Abstract is enclosed herein to replace the original Abstract filed with the application. It is believed that this amendment does not introduce new matter in the application. Therefore, it is respectfully submitted that the objection to the specification should be withdrawn.

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner stated that the recitation of claim 1 is unclear as to which element contacts the top surface of the GaAs wafer and supports both sides of the wafer and what sides of the wafer are supported. Claim 1 has been amended to particularly point out and distinctly claim the subject matter in accordance with accepted U.S. practice. Therefore, it is respectfully requested that this rejection be withdrawn.

Claim 1 was also rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,974,039 issued to Schindler, et. al. (hereinafter referred to as "the Schindler reference"). The Examiner stated that in part that, although the Schindler reference does not disclose a π – structured gate, this limitation is taken to be a product by process limitation since the Schindler reference does disclose an air bridge layer. The Examiner further stated that since the Schindler reference discloses a product that "appears to be identical with or only slightly different than the product claimed," a rejection under § 103 is proper.

The Schindler reference discloses a field effect transistor having at least one integrated capacitor. The transistor includes drain and source contacts disposed over a semi-insulating substrate comprised of gallium arsenide (GaAs). In an embodiment referred to by the Examiner, source contacts are coupled by an overlay metallization to one of a pair of pads having via holes which couples said overlay metallization to a ground plane conductor. In addition, portions of the overlay metallization provide air bridges over gate electrodes, which are disposed between respective pairs of source and drain electrodes.

Claim 1, as amended, recites, in part, a gate having a π structure and formed using an air bridge technique over the top surface of the GaAs wafer so as to contact the GaAs wafer between each source layer and the drain, thereby supporting the laterally opposite ends of the

GaAs wafer over the air layer and the drain. The Schindler reference does not teach or suggest a π – structured gate. The invention as described in amended claim 1 relates to improve a frequency characteristic and a reduction of gate resistance by connecting two gates to each other through an air bridge structure. This is in order to overcome any limitation created by the inability to widen the gate head as a result of the sizes of the source and drain in a conventional gate structure. The Schindler reference however suggests connecting source layers by an air bridge structure to improve element character.

The Schindler reference teaches a gate structure that encompasses not only the drain but the source portions as well. Amended claim 1 of the present invention describes a gate structure formed over the drain 5 only. Therefore, the Schindler reference teaches away from the present invention. In addition, the source contacts in the Schindler reference are coupled to the GND by the overlay metallization (gate structure), whereas, in the present invention, the source contacts are directly in contact with the GND as a result of the process of back-side via holes. Further, the gate layer in the Schindler reference does not "contact the substrate between the first and second source layers and the drain" as recited in amended claim 1. Consequently, the differing gate structures between the present invention and that disclosed in the Schindler reference, and the resulting characteristics of the respective transistors, render the present invention patently distinct from the Schindler reference. Therefore, claim 1, as amended, distinguishes over the Schindler reference and this rejection should be withdrawn.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein; and no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California, telephone number (213) 250-7780 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,
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Date: January 2, 2003

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